WHAT IS CLAIMED IS:

1. A memory compiler characterization method for determining parametric data associated with compilable memory instances, comprising the steps:

obtaining a first parametric dataset for a first plurality of memory compilers, each of said memory compilers for compiling a respective memory instance having a select number of physical rows and a select number of physical columns, wherein each memory instance is organized using a first MUX factor and each data point in said first parametric dataset corresponds to said respective memory instance, said data point comprising a value with respect to a particular parameter;

obtaining a second parametric dataset by characterizing said particular parameter for a second plurality of memory compilers, each of said second plurality of memory compilers for compiling a respective memory instance organized with a second MUX factor, wherein said second plurality of memory compilers are sampled from said first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds to a respective congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns;

determining scale factors for a select number of parametric data points associated with respective

congruent memory instances of said first and second parametric datasets;

obtaining an interpolated scale factor based on said scale factors; and

deriving a value of said particular parameter for an additional memory instance of second parametric dataset by applying said interpolated scale factor to a data point associated with a memory instance of said first parametric dataset, wherein said memory instance is congruent with respect to said additional memory instance of said second parametric dataset.

2. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said particular parameter comprises a memory timing parameter.

3. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 2, wherein said memory timing parameter comprises memory access time.

4. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 2, wherein said memory timing parameter comprises memory cycle time.

5. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said first MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

6. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said second MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

7. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein each memory instance of said first and second parametric datasets comprises a read-only memory (ROM) circuit.

8. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein each memory instance of said first and second parametric datasets comprises a static random access memory (SRAM) circuit.

9. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein each memory instance of said first and second parametric datasets comprises a dynamic random access memory (DRAM) circuit.

10. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein each memory instance of said first and second parametric datasets comprises an electrically programmable ROM (EPROM) circuit.

11. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein each memory instance of said first and second parametric datasets comprises a flash memory circuit.

12. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein each memory instance of said first and second parametric datasets comprises an embedded memory circuit.

13. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein each memory instance of said first and second parametric datasets comprises a stand-alone memory circuit.

14. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said interpolated scale factor is obtained by interpolating four scale factors, each corresponding to a ratio of values of said particular parameter for a pair of congruent memory instances.

15. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 1, wherein said step of obtaining said first parametric dataset and said step of obtaining said second parametric dataset are effectuated by characterization of said particular parameter via simulation.

16. A memory compiler characterization method for determining parametric data associated with compilable memory instances, comprising the steps:

obtaining a first parametric dataset for a first plurality of memory compilers representative of a first memory technology, each of said memory compilers for compiling a respective memory instance having a select number of physical rows and a select number of physical columns and organized using a select MUX factor, wherein each data point in said first parametric dataset corresponds to said respective memory instance, said data point comprising a value with respect to a particular parameter;

obtaining a second parametric dataset by characterizing said particular parameter for a second plurality of memory compilers that are representative of a second memory technology, each of said second plurality of memory compilers for compiling a respective memory instance organized with said select MUX factor, wherein said second plurality of memory compilers are sampled from said first plurality of memory compilers such that each memory instance compiled by said second plurality of memory compilers corresponds to a respective congruent memory instance of said first parametric dataset having identical numbers of physical rows and physical columns;

determining scale factors for a select number of parametric data points associated with respective

congruent memory instances of said first and second parametric datasets;

obtaining an interpolated scale factor based on said scale factors; and

deriving a value of said particular parameter for an additional memory instance of second parametric dataset by applying said interpolated scale factor to a data point associated with a memory instance of said first parametric dataset, wherein said memory instance is congruent with respect to said additional memory instance of said second parametric dataset.

17. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said particular parameter comprises a memory timing parameter.

18. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 17, wherein said memory timing parameter comprises memory access time.

19. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 17, wherein said memory timing parameter comprises memory cycle time.

20. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said select MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

21. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein each memory instance of said first and second parametric datasets comprises a read-only memory (ROM) circuit.

22. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein each memory instance of said first and second parametric datasets comprises a static random access memory (SRAM) circuit.

23. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein each memory instance of said first and second parametric datasets comprises a dynamic random access memory (DRAM) circuit.

24. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein each memory instance of said first and second parametric datasets comprises an electrically programmable ROM (EPROM) circuit.

25. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein each memory instance of said first and second parametric datasets comprises a flash memory circuit.

26. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein each memory instance of said first and second parametric datasets comprises an embedded memory circuit.

27. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein each memory instance of said first and second parametric datasets comprises a stand-alone memory circuit.

28. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said interpolated scale factor is obtained by interpolating four scale factors, each corresponding to a ratio of values of said particular parameter for a pair of congruent memory instances.

29. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said step of obtaining said first parametric dataset and said step of obtaining said second parametric dataset are effectuated by characterization of said particular parameter via simulation.

30. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said first memory technology is selected from the group consisting of 1.0μ technology, 0.8μ technology, 0.6μ technology and 0.2μ technology.

31. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said second memory technology is selected from the group consisting of 1.0μ technology, 0.8μ technology, 0.6μ technology and 0.2μ technology.

32. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said first and second memory technologies comprise design-rule-specific technologies.

33. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said first and second memory technologies comprise foundry-specific technologies.

34. The memory compiler characterization method for determining parametric data associated with compilable memory instances as set forth in claim 16, wherein said first and second memory technologies comprise process-flow-specific technologies.

35. A memory compiler characterization system, comprising:

means for characterizing a first plurality of memory compilers with respect to a particular parameter, said first plurality of memory compilers for compiling memory instances of a first type;

means for characterizing a second plurality of memory compilers with respect to said particular parameter, said second plurality of memory compilers for compiling memory instances of a second type, wherein said memory instances of second type comprise memory instances sparsely sampled from said memory instances of first type such that each memory instance of second type corresponds to a respective congruent memory instance of first type having identical numbers of physical rows and physical columns;

means for determining scale factors between values of said particular parameter respectively associated with a sample of congruent memory instances of said first and second types;

an interpolator to obtain an interpolated scale factor based on said scale factors; and

means for obtaining a value of said particular parameter for an additional memory instance of second type by utilizing said interpolated scale factor in conjunction with a parametric value of a congruent memory instance of first type which corresponds to said additional memory instance.

36. The memory compiler characterization system as set forth in claim 35, wherein said memory instances of first type comprise memory instances with a first MUX factor and said memory instances of second type comprise memory instances with a second MUX factor.

37. The memory compiler characterization system as set forth in claim 36, wherein said first MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

38. The memory compiler characterization system as set forth in claim 36, wherein said second MUX factor is selected from the group consisting of a MUX-4 factor, a MUX-8 factor, a MUX-16 factor and a MUX-32 factor.

39. The memory compiler characterization system as set forth in claim 35, wherein said memory instances of first type comprise memory instances associated with a first memory technology and said memory instances of second type comprise memory instances associated with a second memory technology.

40. The memory compiler characterization system as set forth in claim 39, wherein said first memory technology is selected from the group consisting of 1.0μ technology, 0.8μ technology, 0.6μ technology and 0.2μ technology.

41. The memory compiler characterization system as set forth in claim 39, wherein said second memory technology is selected from the group consisting of 1.0μ technology, 0.8μ technology, 0.6μ technology and 0.2μ technology.

42. The memory compiler characterization system as set forth in claim 39, wherein said first and second memory technologies comprise design-rule-specific technologies.

43. The memory compiler characterization system as set forth in claim 39, wherein said first and second memory technologies comprise process-flow-specific technologies.

44. The memory compiler characterization system as set forth in claim 39, wherein said first and second memory technologies comprise foundry-specific technologies.

45. The memory compiler characterization system as set forth in claim 35, wherein said memory instances comprise one of a DRAM circuit, an SRAM circuit, a ROM circuit, an EPROM circuit and a flash memory circuit.

46. A computer-accessible medium operable in connection with a processor environment, said computer-accessible medium carrying a sequence of instructions which, when executed in said processor environment, cause the following steps to be performed:

characterizing a first plurality of memory compilers with respect to a particular parameter, said first plurality of memory compilers for compiling memory instances of a first type;

characterizing a second plurality of memory compilers with respect to said particular parameter, said second plurality of memory compilers for compiling memory instances of a second type, wherein said memory instances of second type comprise memory instances sparsely sampled from said memory instances of first type such that each memory instance of second type corresponds to a respective congruent memory instance of first type having identical numbers of physical rows and physical columns;

determining scale factors between values of said particular parameter respectively associated with a sample of congruent memory instances of said first and second types;

obtaining an interpolated scale factor based on said scale factors; and

deriving a value of said particular parameter for an additional memory instance of second type by applying said interpolated scale factor in conjunction with a parametric value of a congruent memory instance of

first type which corresponds to said additional memory instance.

47. The computer-accessible medium as set forth in claim 46, wherein said memory instances of first type comprise memory instances with a first MUX factor and said memory instances of second type comprise memory instances with a second MUX factor.

48. The computer-accessible medium as set forth in claim 46, wherein said memory instances of first type comprise memory instances associated with a first memory technology and said memory instances of second type comprise memory instances associated with a second memory technology.

49. The computer-accessible medium as set forth in claim 46, wherein said memory instances comprise one of a DRAM circuit, an SRAM circuit, a ROM circuit, an EPROM circuit and a flash memory circuit.